POSTAL BOOK PACKAGE 2026

ELECTRONICS ENGINEERING

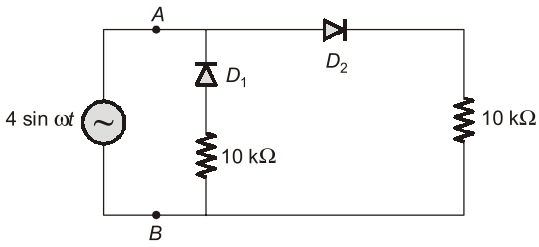
CONVENTIONAL Practice Sets

CONTENTS

ANALOG CIRCUITS

1 CHAPTER
Diode Circuits

Q.1 A voltage source $V_{AB} = 4 \sin \omega t$, is applied across the terminals A and B of the circuit. The diodes are assumed to be ideal. Find the impedance offered by the circuit across the terminals A and B in kilo ohm.



Solution:

In +ve half cycle D_1 – off (R.B.)

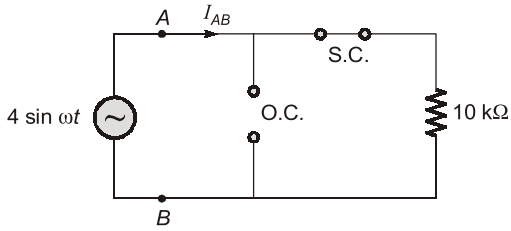
D_2 – on (F.B.)

$\therefore$ Equivalent circuit will be

$\therefore$ $V_{AB} = 4 \sin \omega t$

$$I_{AB} = \frac{V_{AB}}{10\,\text{k}\Omega}$$

$\therefore$ $$R_i = \frac{V_{AB}}{I_{AB}} = 10\text{k}\Omega$$



For –ve half cycle,

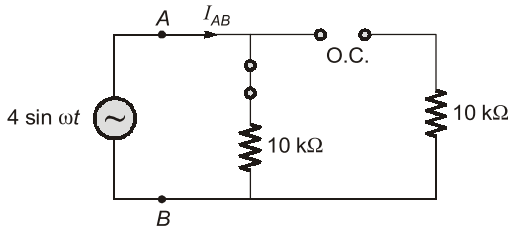
D_1 on, D_2 off

Equivalent circuit,

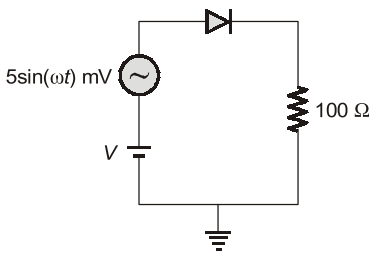
$V_{AB} = 4 \sin \omega t$

$$I_{AB} = \frac{4 \sin \omega t}{10\,\text{k}\Omega}$$

$\therefore$ $$\frac{V_{AB}}{I_{AB}} = R_i = 10\ \text{k}\Omega$$



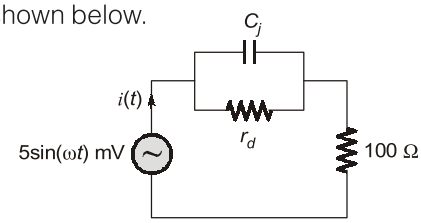
Q.2 A DC current of 26 μA flows through the circuit shown. The diode in the circuit is forward biased and it has an ideality factor of one. At the quiescent point, the diode has a junction capacitance of 0.5 nF. Its neutral region resistances can be neglected. Assume that the room temperature thermal equivalent voltage is 26 mV.



For $\omega = 2 \times 10^6$ rad/s, the amplitude of the small-signal component of diode current.

Solution:

The small-signal equivalent model of the given circuit can be drawn as shown below.



Given that,

$\omega = 2 \times 10^6$ rad/sec

$C_j = 0.5$ nF

$I_{DC} = 26$ μA

$V_T = 26$ mV

$\eta = 1$

Since, small signal incremental diode resistance, $r_d = \dfrac{\eta V_T}{I_{DC}} = \dfrac{26\text{ mV}}{26\ \mu\text{A}} = 1\text{k}\Omega$

and impedance due to junction capacitance, $\dfrac{1}{\omega C_j} = \dfrac{1}{2\times10^6 \times 0.5 \times 10^{-9}}\ \Omega = 1\text{k}\Omega$

So, total impedance of the circuit will be,

$$Z = \left(r_d \| \frac{1}{j\omega C_j}\right) + 100\ \Omega$$

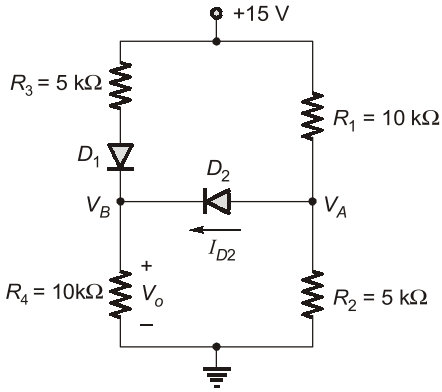
$$\left(r_d \| \frac{1}{j\omega C_j}\right) = \frac{(1000)(-j1000)}{1000 - j1000}\ \Omega = \frac{-j(1+j)}{2}\ \text{k}\Omega = \frac{1}{2}(1-j)\ \text{k}\Omega = (500 - j500)\ \Omega$$

$\therefore$ $Z = 600 - j500\ \Omega$

$|Z| = 100\sqrt{36+25} = 100\sqrt{61}\ \Omega$

$$I_m = \frac{V_m}{|Z|} = \frac{5\text{ mV}}{100\sqrt{61}\ \Omega} = \frac{50}{\sqrt{61}}\ \mu\text{A} = 6.40\ \mu\text{A}$$

Q3 Determine the current I_{D2} and the voltage V_o in the multidiode circuit shown in the figure below. Assume that, cut-in voltage $V_\gamma = 0.7$ V for each diode.



Solution:

To begin, initially assume that, both the diodes D_1 and D_2 are in their conducting state.

By applying KCL at A and B nodes, we have

$$\frac{15 - V_A}{10} = I_{D2} + \frac{V_A}{5} \qquad \text{...(i)}$$

and $$\frac{15 - (V_B + 0.7)}{5} + I_{D2} = \frac{V_B}{10} \qquad \text{...(ii)}$$

We note that $V_B = V_A - 0.7$. Combining the two equations and eliminating I_{D2}, we find

$V_A = 7.62$ V and $V_B = 6.92$ V

From equation (i) above, we obtain

$$\frac{15-7.62}{10} = I_{D2} + \frac{7.62}{5} \Rightarrow I_{D2} = -0.786\ \text{mA}$$

We assumed that D_2 was ON, so a negative current is inconsistent with that initial assumption.
Now assume that diode D_2 is OFF and D_1 is ON. To find the node voltages, we can simply use voltage divider principle as

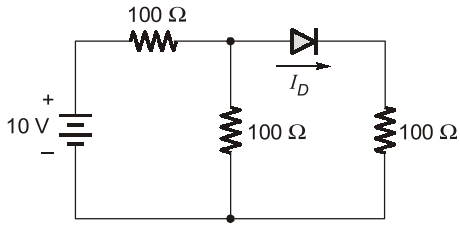
$$V_A = \left(\frac{5}{5+10}\right)(15) = 5\ \text{V}$$

and

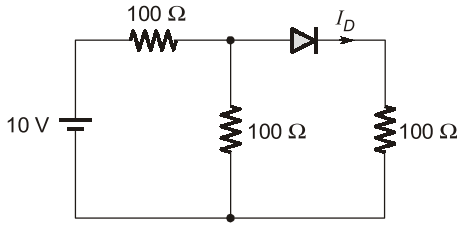
$$V_B = V_O = \left(\frac{10}{10+5}\right)(15-0.7) = 9.53\ \text{V}$$

These voltages show that diode D_2 is indeed reverse biased so that $I_{D2} = 0$.

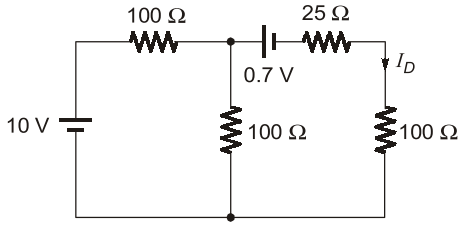
Q4 **Find the diode current I_D in the circuit shown below when the diode has cut in voltage, $V_\gamma = 0.7$ V and forward resistance, $R_f = 25\ \Omega$.**

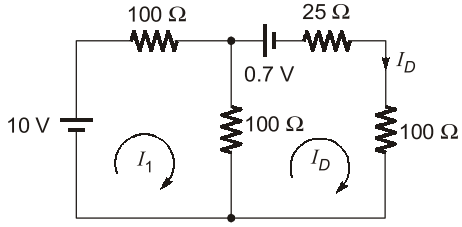


Solution:



Given : Diode cut-in voltage = 0.7 V and diode forward resistance = 25 Ω
Replacing the diode with its equivalent, we get,





Using KVL, $10 - 100I_1 - 100(I_1 - I_D) = 0$ ...(i)

$$-0.7 - 125I_D + 100(I_1 - I_D) = 0 \quad \text{...(ii)}$$

Solving equation (i) and (ii)

$$10 - 200I_1 - 100I_D = 0 \quad \text{...(iii)}$$

$$-0.7 - 225I_D + 100I_1 = 0 \quad \text{...(iv)}$$

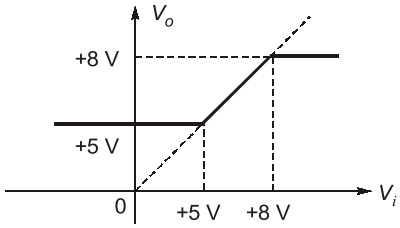
Multiplying equation (iv) by 2 and adding, we get

$$10 - 1.4 - 450I_D - 100I_D = 0$$

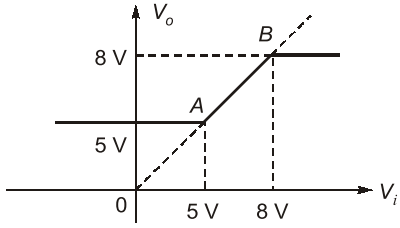
$$8.6 = 550I_D$$

$$\therefore \quad I_D = \frac{8.6}{550} = 15.63\ \text{mA}$$

Q.5 The ideal transfer characteristic of a particular circuit is given in figure. Design the circuit. Draw the output waveform with proper explanation, if $V_i = 10 \sin \omega t$.



Solution:



Slope of the curve between A and B is

$$m = \frac{(8-5)}{(8-5)} = 1$$

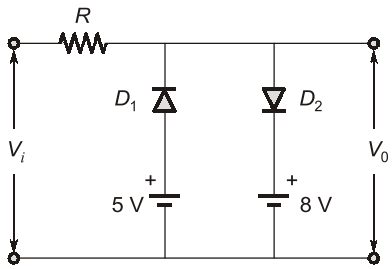
The circuit diagram for the above input-output (transfer) characteristic is a two-level clipper as shown below.

Cut in voltages of diodes are zero.

For $V_i < 5$ V $\rightarrow$ diode D_1 will be on and D_2 will be off

and $\boxed{V_0 = 5 \text{ V}}$

For $V_i > 8$ V $\rightarrow$ diode D_1 will be off and diode D_2 will be on



and $\boxed{V_0 = 8 \text{ V}}$

For $5 < V_i < 8$ V $\rightarrow$ both the diodes will be off

and $\boxed{V_0 = V_i}$

Given that $V_i = 10 \sin \omega t$

or $V_i = 10 \sin\theta$ $(\omega t = \theta)$

For $V_i < 5$; $10\sin\theta < 5 \Rightarrow 0 < \theta < 30°$ and $150° < \theta < 360°$

$V_o = 5$ V

For $V_i > 8$ V; $10\sin\theta > 8 \Rightarrow 53.13° < \theta < 126.869°$

$V_o = 8$ V

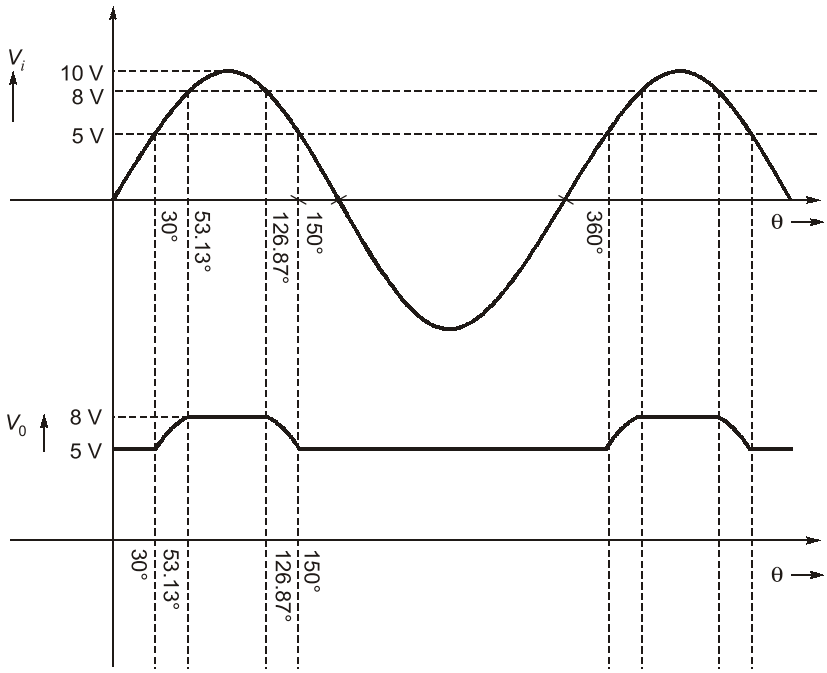
For $5 < V_i < 8$ V; $30° < \theta < 53.13°$ and $126.87° < \theta < 150°$

$V_o = V_i$

The required voltage-current characteristics can be written as

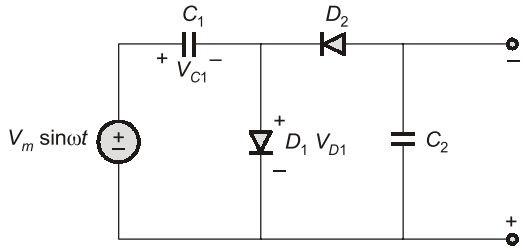
$$V_o = \begin{cases} 5 \text{ V} & ; \quad V_i < 5 \text{ V} \\ V_i & ; \quad 5 \text{ V} < V_i < 8 \text{ V} \\ 8 \text{ V} & ; \quad V_i > 8 \text{ V} \end{cases}$$

Now output waveform will be

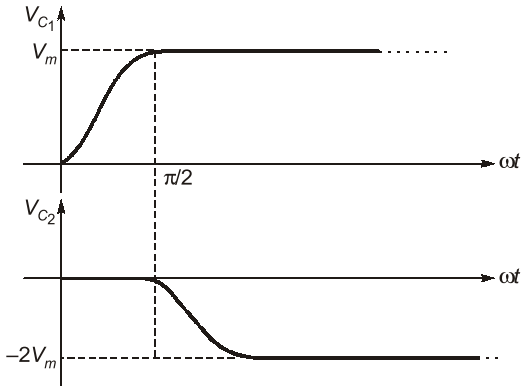


Q.6 Draw the neat circuit of a voltage doubler. Explain its operation. Draw the waveforms for the voltages across the two capacitors.

Solution:



The figure shows a circuit-composed of two sections in cascade, a clamp circuit formed by C_1 and D_1 and peak rectifier formed by D_2 and C_2.



When excited by a sinusoidal of amplitude V_m the clamping section provides the waveform shown. Assuming ideal diodes, while the positive peaks are damped to 0 V, the negative peak reaches $-2V_m$. In response to this wave form, the peak-detector section provides, across capacitor C_2 a negative dc voltage of magnitude $2V_m$. Because the output voltage is double the input peak, the circuit is known as a voltage doubler.